Flat-Panel Display Backplanes: Past, Present, and a Possible Future Option

SID PNW Chapter

Corvallis, OR

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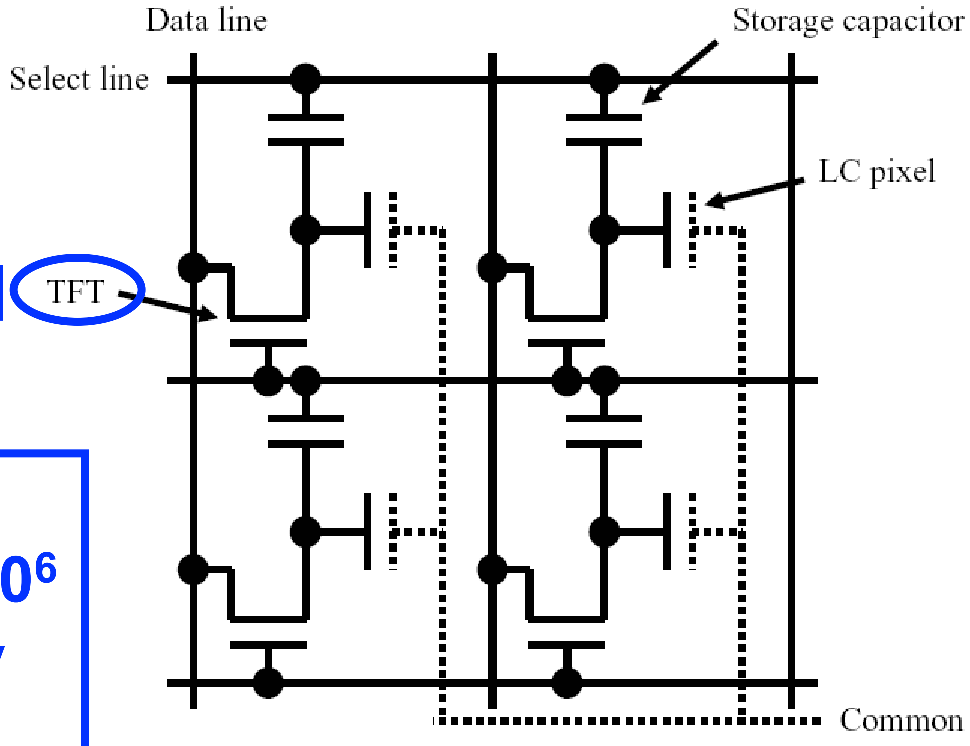
(i) Past

AMLCD backplane



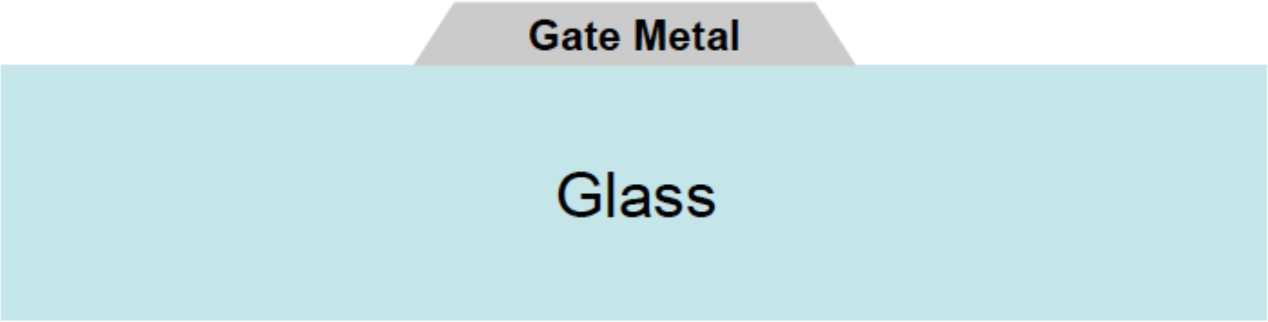
***Switching transistor*:**

- **on-to-off ratio ≥ 10^6**
- **manufacturability**
- ***voltage-control***
- **mobility (…)**
- **stability (…)**

a-Si:H

Backplane Process Flow

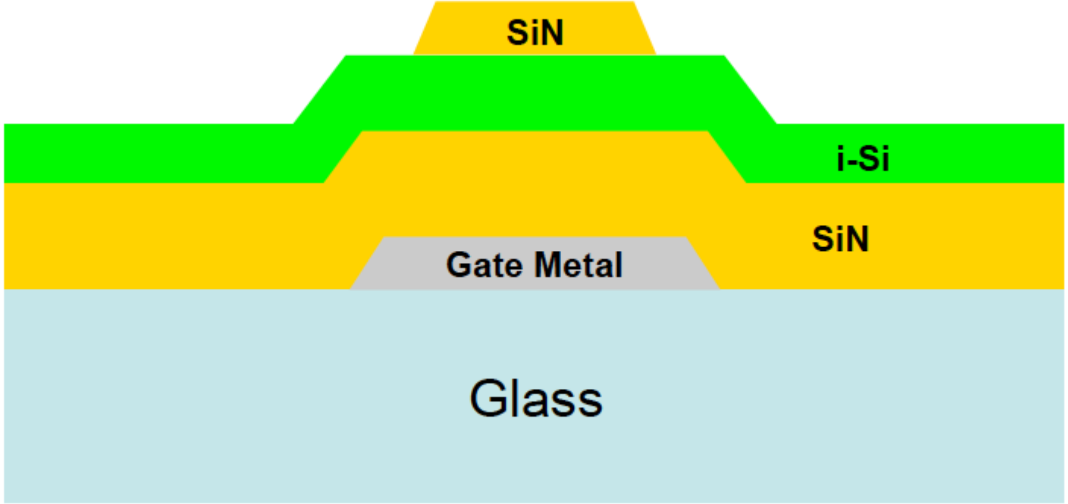
I. a-Si:H TFT Etch-Stop (ES)



1. Deposition and definition of metal gate (**M1**)

Backplane Process Flow

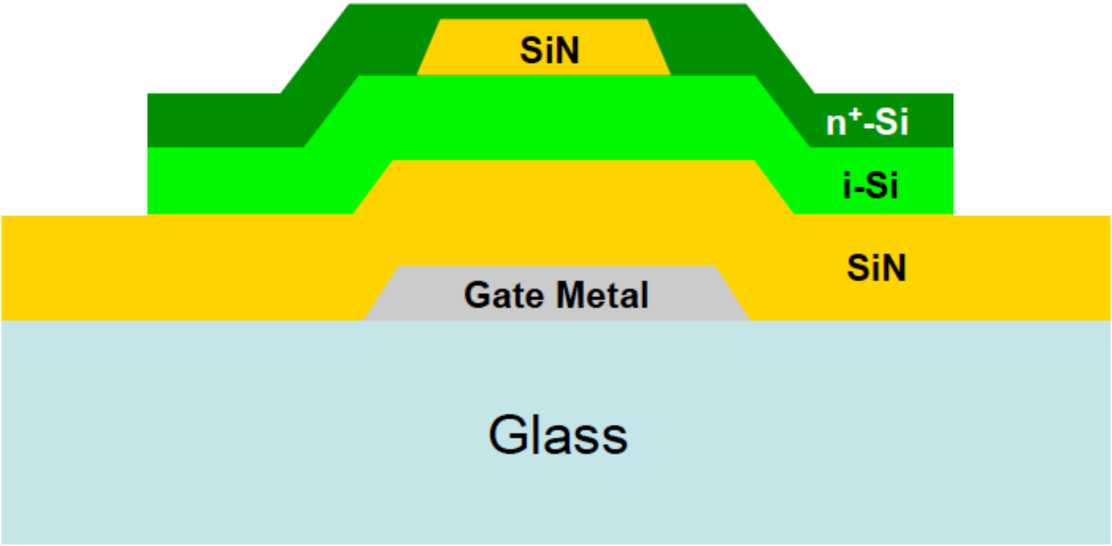
I. a-Si:H TFT Etch-Stop (ES)



2. Sequential deposition of SiN gate dielectric, i a-Si:H, and SiN etch-stop layer
3. Definition of SiN etch stop pad (**M2**)

Backplane Process Flow

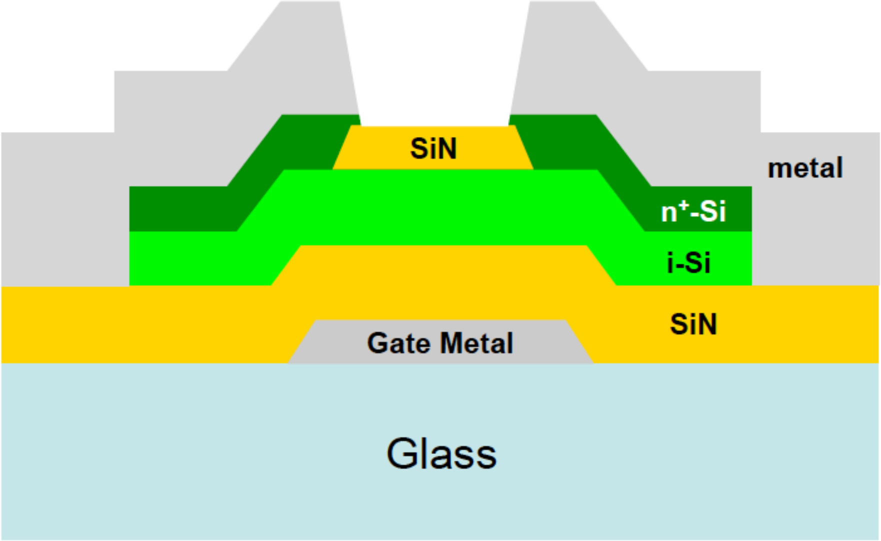
I. a-Si:H TFT Etch-Stop (ES)



4. Deposition of n^+ a-Si:H
5. Definition of TFT island (**M3**)

Backplane Process Flow

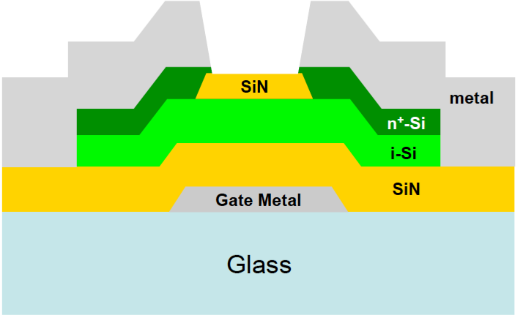
I. a-Si:H TFT Etch-Stop (ES)



6. Deposition and definition of metal S, D contacts (**M4**) and removal of n^+ a-Si:H
7. Deposition of final passivation layer and contact window opening to S, D, and G metals (**M5**)

Backplane Process Flow

I. a-Si:H TFT Etch-Stop (ES)



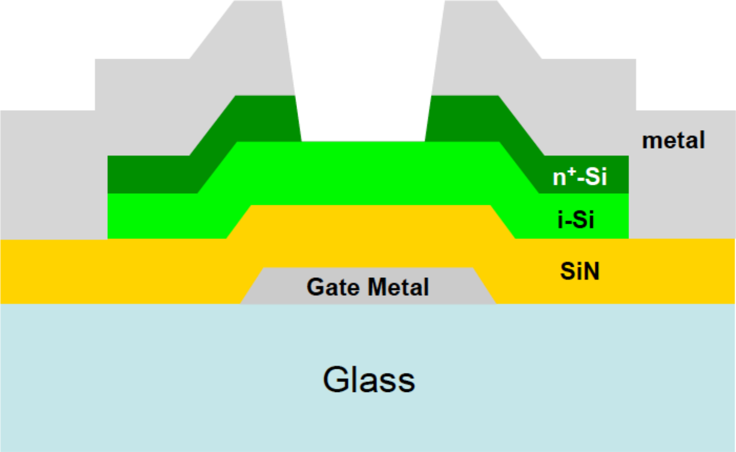
M5

I. a-Si:H TFT Etch-Stop (ES) Process Flow

1. Deposition and definition of metal gate (**M1**)
2. Sequential deposition of SiN gate dielectric, i a-Si:H, and SiN etch-stop layer
3. Definition of SiN etch stop pad (**M2**)
4. Deposition of n^+ a-Si:H
5. Definition of TFT island (**M3**)
6. Deposition and definition of metal S, D contacts (**M4**) and removal of n^+ a-Si:H
7. Deposition of final passivation layer and contact window opening to S, D, and G metals (**M5**)

Backplane Process Flow

II. a-Si:H TFT Back-Channel Etch (BCE)



M4

II. a-Si:H TFT Back-Channel Etch (BCE) Process Flow

1. Deposition and definition of metal gate (**M1**)
2. Sequential deposition of SiN gate dielectric, i a-Si:H, and n^+ a-Si:H
3. Definition of a-Si TFT island (**M2**)
4. Deposition and definition of metal S, D contacts (**M3**)
5. Etch back of exposed n+ a-Si:H (over-etch to ensure clearance)
6. Deposition of final passivation layer and contact window opening to S, D, and G metals (**M4**)

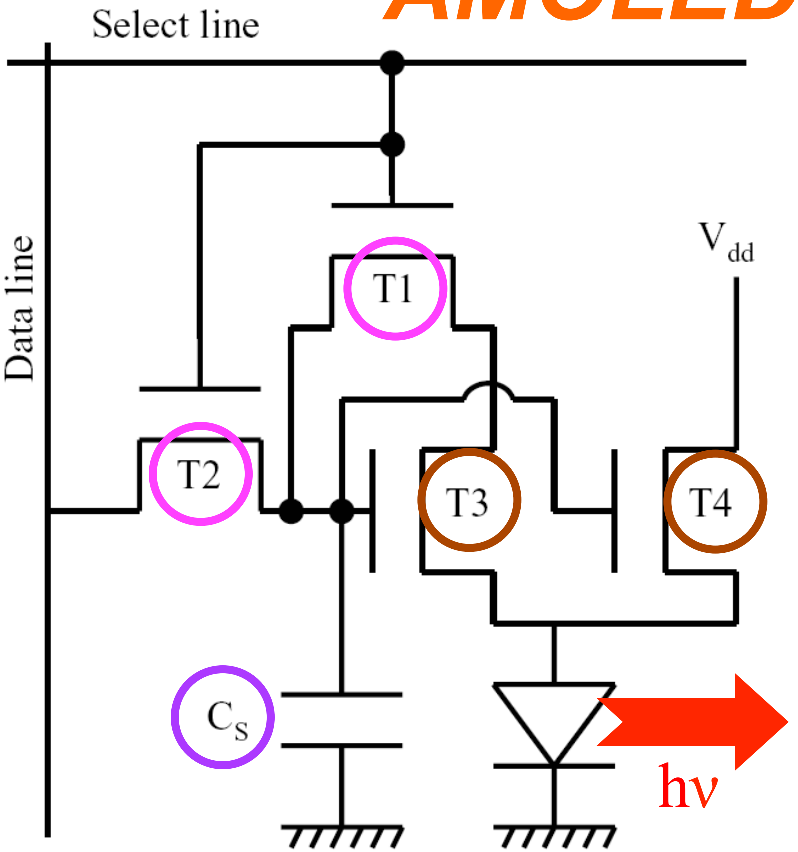
(ii) Present

Larger and/or higher resolution AMLCD displays require a backplane semiconductor with a higher mobility!

Display Backplane Options

Property	**a-Si:H**	**LTPS**	**IGZO**
Microstructure	amorphous	polycrystalline	amorphous
V_T uniformity	good	fair*	fair*
V_T stability	poor	good	fair
Mobility ($cm^2V^{-1}s^{-1}$)	~ 1	~ 50-100	~ 10-30
Mobility Uniformity	good	fair*	fair*
Device type	NMOS	CMOS	NMOS
Process complexity	low	high	low

AMOLED backplane



Switching & Drive transistors:

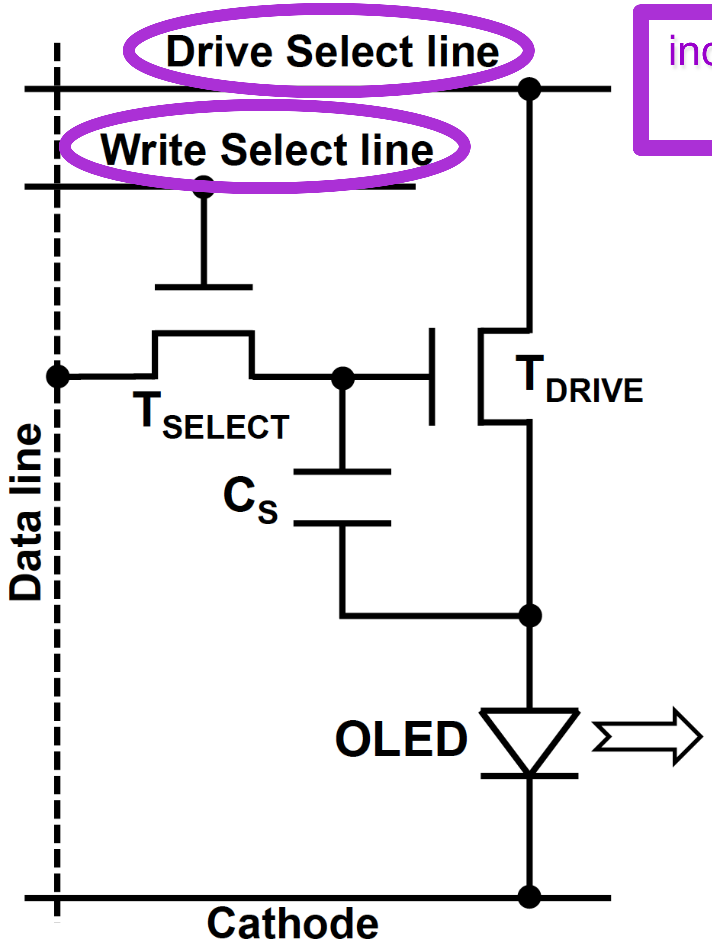
- **manufacturability**
- ***current-control***
- **mobility (!!)**
- **stability (!!!)**

Compensate for:

- **OLED instability**
- **TFT instability**
- **TFT V_T, μ nonuniformity**

C. Church and A. Nathan, Information Display 3&4/05, 22 (2005).

AMOLED backplane (best case)



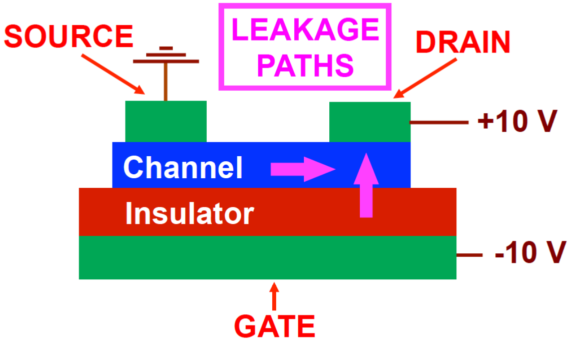
independent control

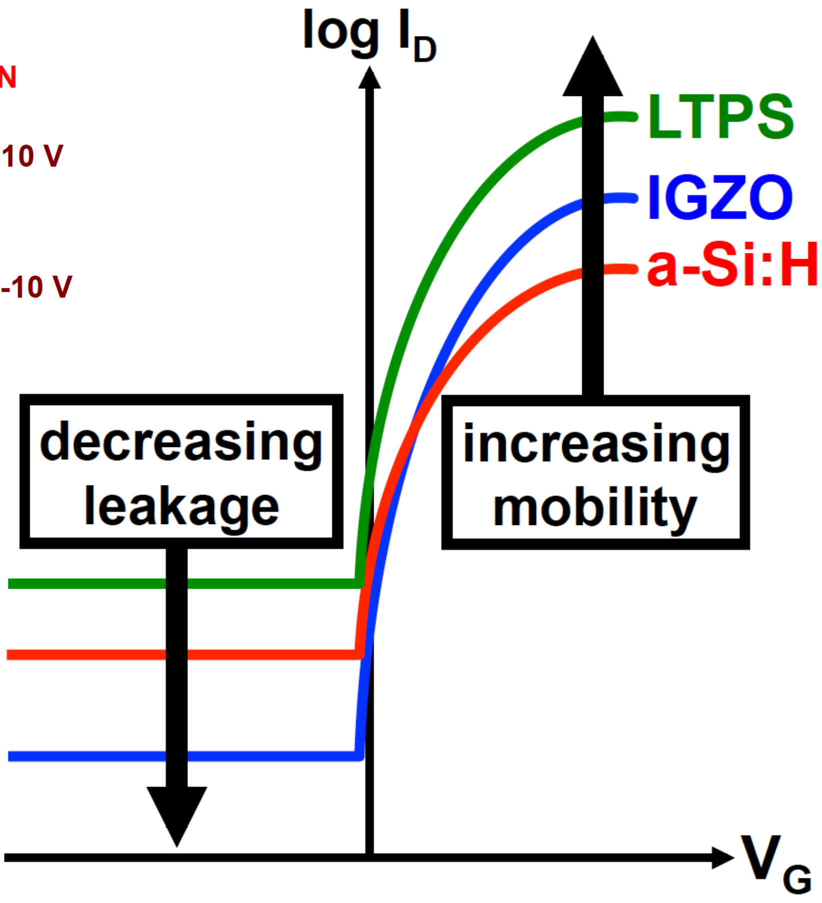
T. Arai, J. SID 20, 156 (2012).

Mobility is not the whole story.

Off current and process complexity also matter!

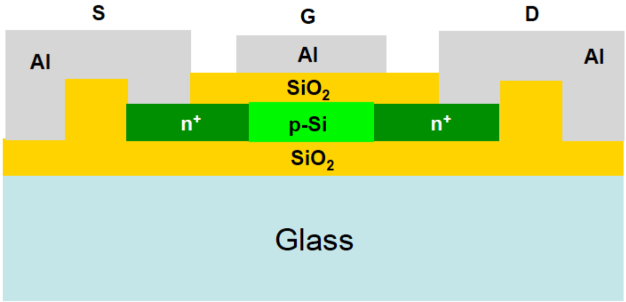
Mobility versus Off Current





Backplane Process Flow

III. LTPS nMOS



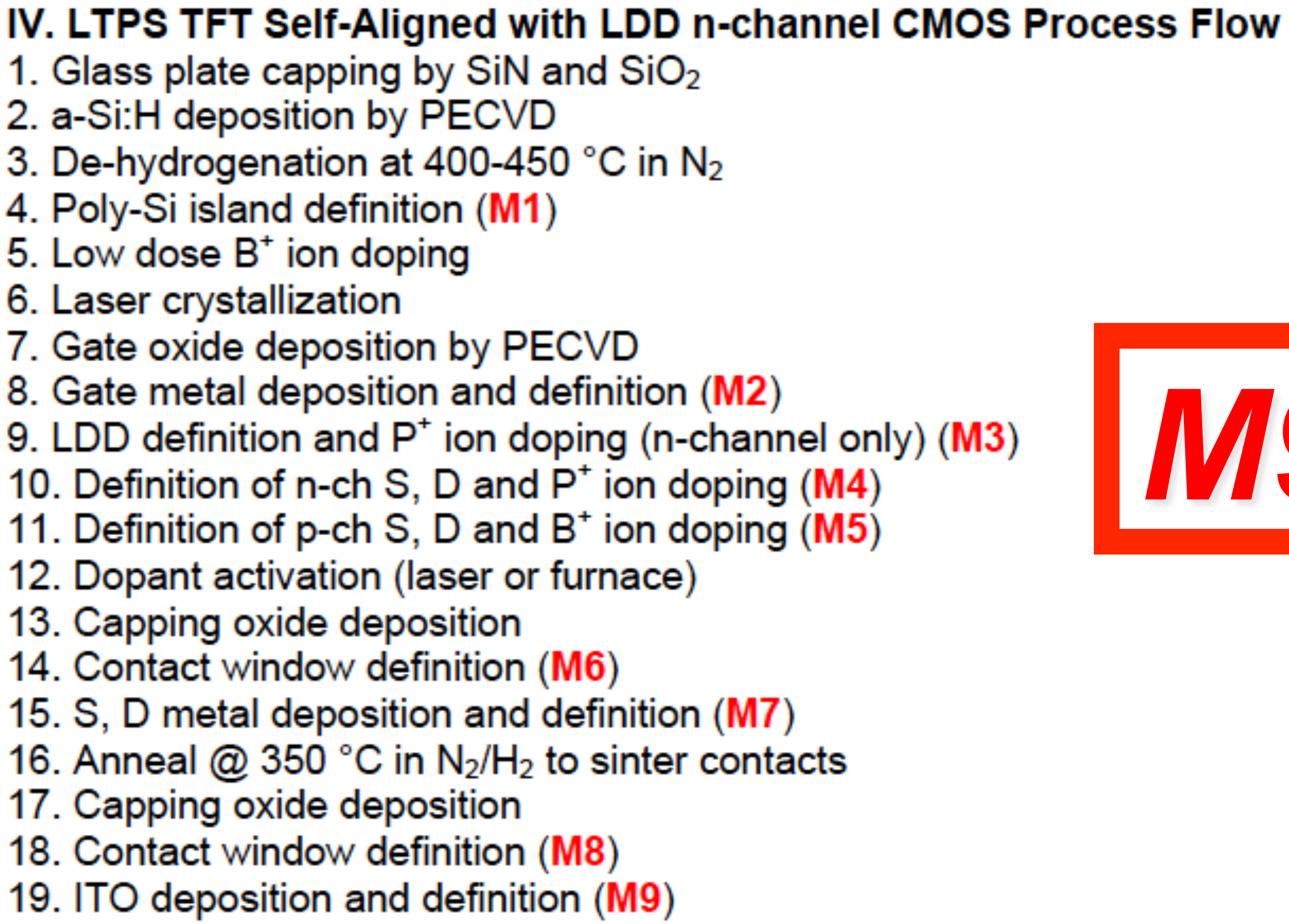
III. LTPS TFT Non-Self-Aligned n-channel Process Flow

1. Glass plate capping by SiN and SiO$_2$
2. a-Si:H deposition by PECVD
3. De-hydrogenation at 400-450 °C in N$_2$
4. Poly-Si island definition (**M1**)
5. Low dose B$^+$ ion doping
6. S, D definition and P$^+$ ion doping (**M2**)
7. Laser crystallization
8. Gate oxide deposition by PECVD
9. Contact window definition (**M3**)
10. S, D, and G metal deposition and definition (**M4**)
11. Anneal @ 350 °C in N$_2$/H$_2$ to sinter contacts

M4

Backplane Process Flow

IV. LTPS CMOS



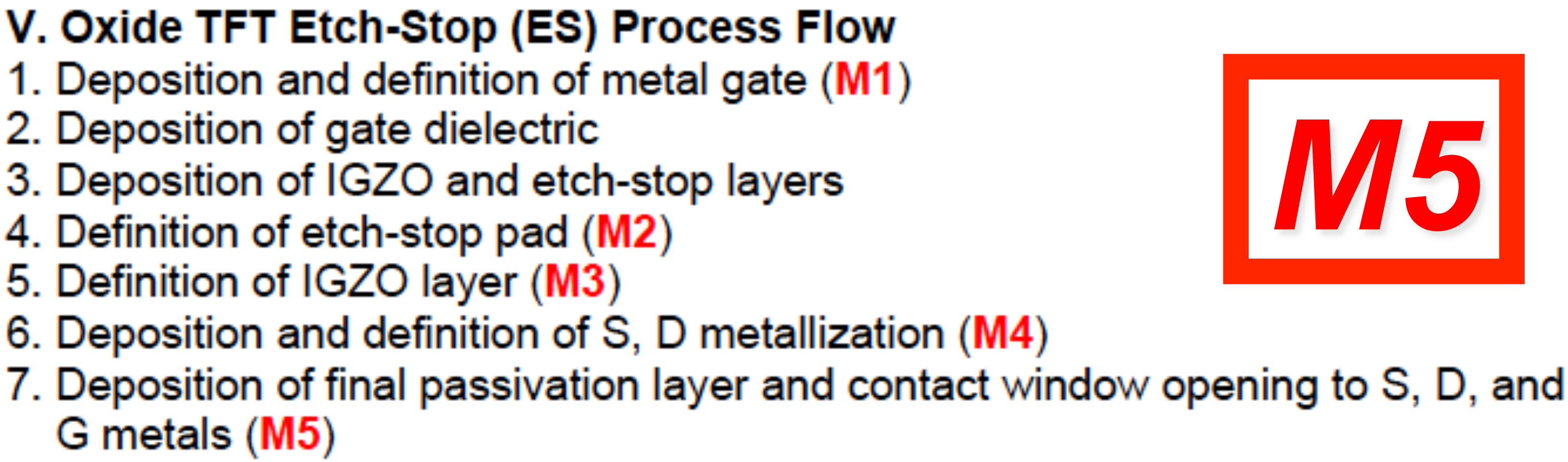
IV. LTPS TFT Self-Aligned with LDD n-channel CMOS Process Flow

1. Glass plate capping by SiN and SiO_2
2. a-Si:H deposition by PECVD
3. De-hydrogenation at 400-450 °C in N_2
4. Poly-Si island definition (**M1**)
5. Low dose B^+ ion doping
6. Laser crystallization
7. Gate oxide deposition by PECVD
8. Gate metal deposition and definition (**M2**)
9. LDD definition and P^+ ion doping (n-channel only) (**M3**)
10. Definition of n-ch S, D and P^+ ion doping (**M4**)
11. Definition of p-ch S, D and B^+ ion doping (**M5**)
12. Dopant activation (laser or furnace)
13. Capping oxide deposition
14. Contact window definition (**M6**)
15. S, D metal deposition and definition (**M7**)
16. Anneal @ 350 °C in N_2/H_2 to sinter contacts
17. Capping oxide deposition
18. Contact window definition (**M8**)
19. ITO deposition and definition (**M9**)

M9

Backplane Process Flow

V. Oxide TFT Etch-Stop (ES)



V. Oxide TFT Etch-Stop (ES) Process Flow

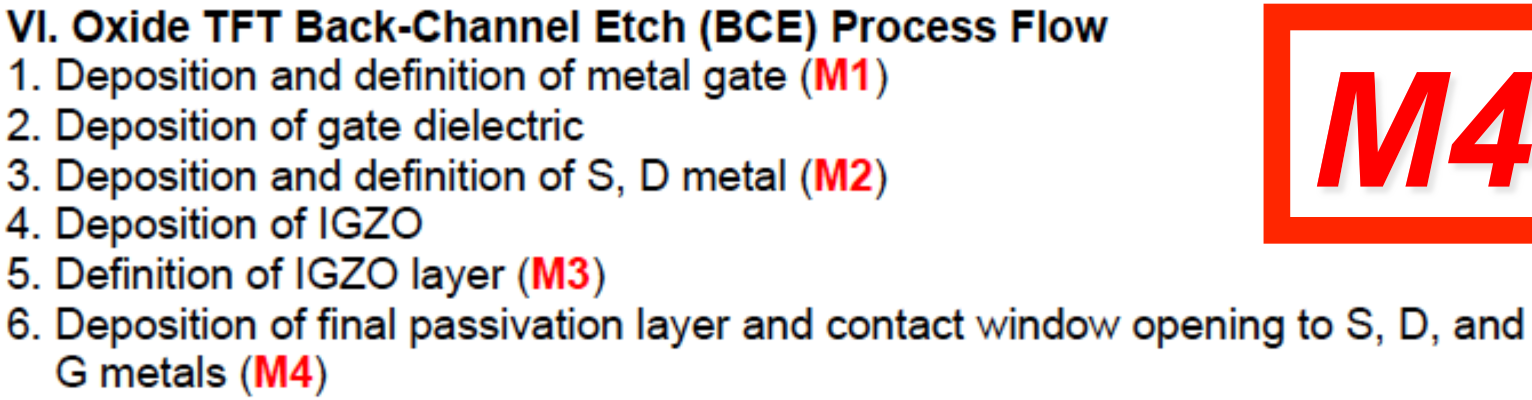
1. Deposition and definition of metal gate (**M1**)
2. Deposition of gate dielectric
3. Deposition of IGZO and etch-stop layers
4. Definition of etch-stop pad (**M2**)
5. Definition of IGZO layer (**M3**)
6. Deposition and definition of S, D metallization (**M4**)
7. Deposition of final passivation layer and contact window opening to S, D, and G metals (**M5**)

M5

Past…

Backplane Process Flow

VI. Oxide TFT Back-Channel Etch (BCE)



VI. Oxide TFT Back-Channel Etch (BCE) Process Flow

1. Deposition and definition of metal gate (**M1**)
2. Deposition of gate dielectric
3. Deposition and definition of S, D metal (**M2**)
4. Deposition of IGZO
5. Definition of IGZO layer (**M3**)
6. Deposition of final passivation layer and contact window opening to S, D, and G metals (**M4**)

M4

Present…

Backplane Process Flow

III. LTPS nMOS

M4

III. LTPS TFT Non-Self-Aligned n-channel Process Flow

1. Glass plate capping by SiN and SiO_2
2. a-Si:H deposition by PECVD
3. De-hydrogenation at **400-450 °C** in N_2
4. Poly-Si island definition (**M1**)
5. Low dose B^+ **ion doping**
6. S, D definition and P^+ **ion doping** (**M2**)
7. **Laser crystallization**
8. Gate oxide deposition by PECVD
9. Contact window definition (**M3**)
10. S, D, and G metal deposition and definition (**M4**)
11. Anneal @ 350 °C in N_2/H_2 to sinter contacts

A bit more on:
Oxide TFTs
or
IGZO

Amorphous oxide semiconductors (AOS)

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

H. Hosono *et al.*, J. Non-Crystalline Solids 203, 334 (1996).

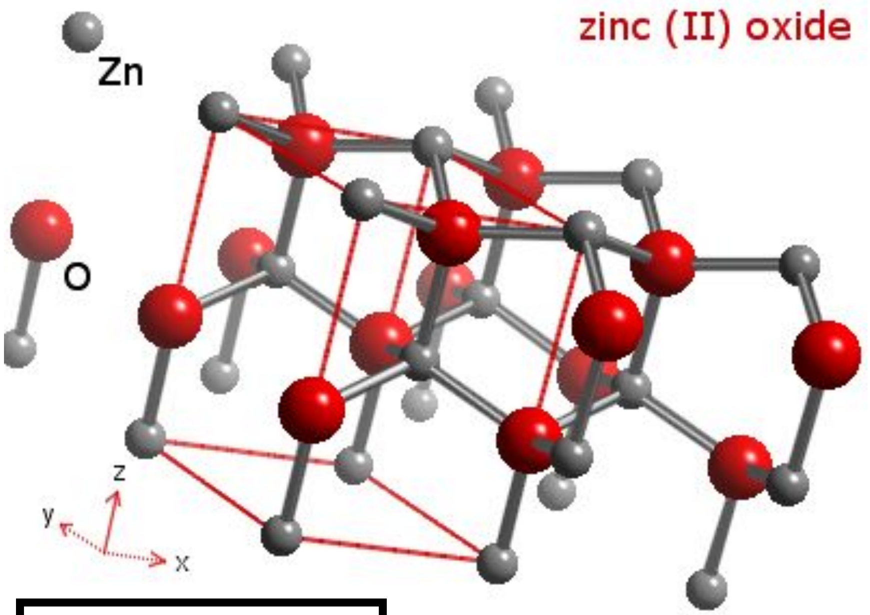
Amorphous oxide semiconductors (AOS)

11 12 13 14 15

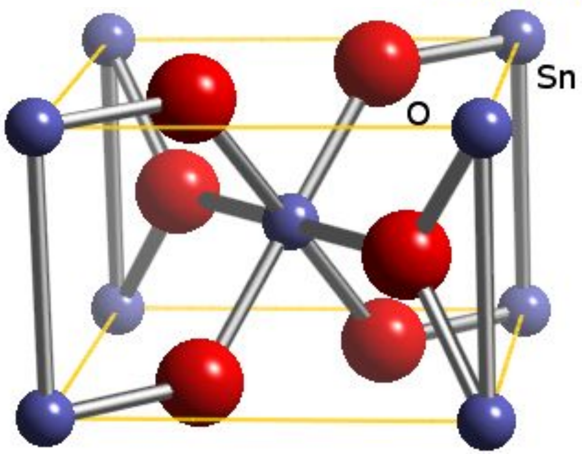
IGZO!

H. Hosono *et al.*, J. Non-Crystalline Solids 203, 334 (1996).

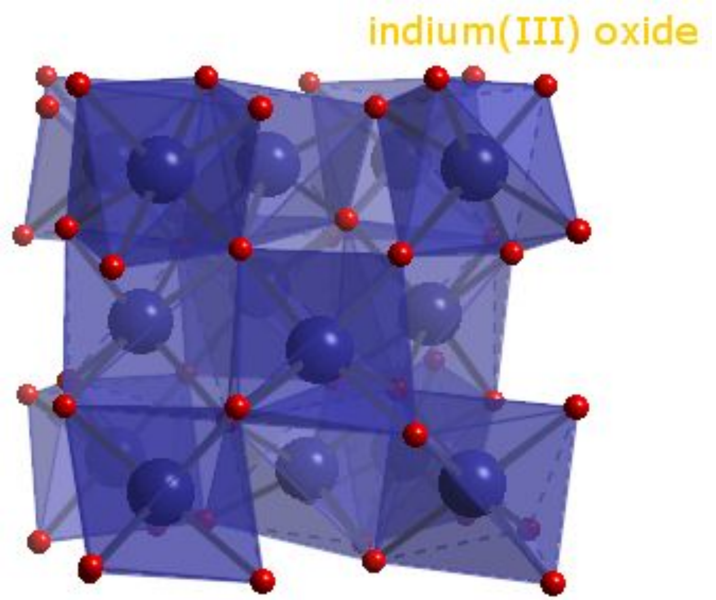
In, Sn, Zn - AOS Stalwarts



ZnO hexagonal wurtzite

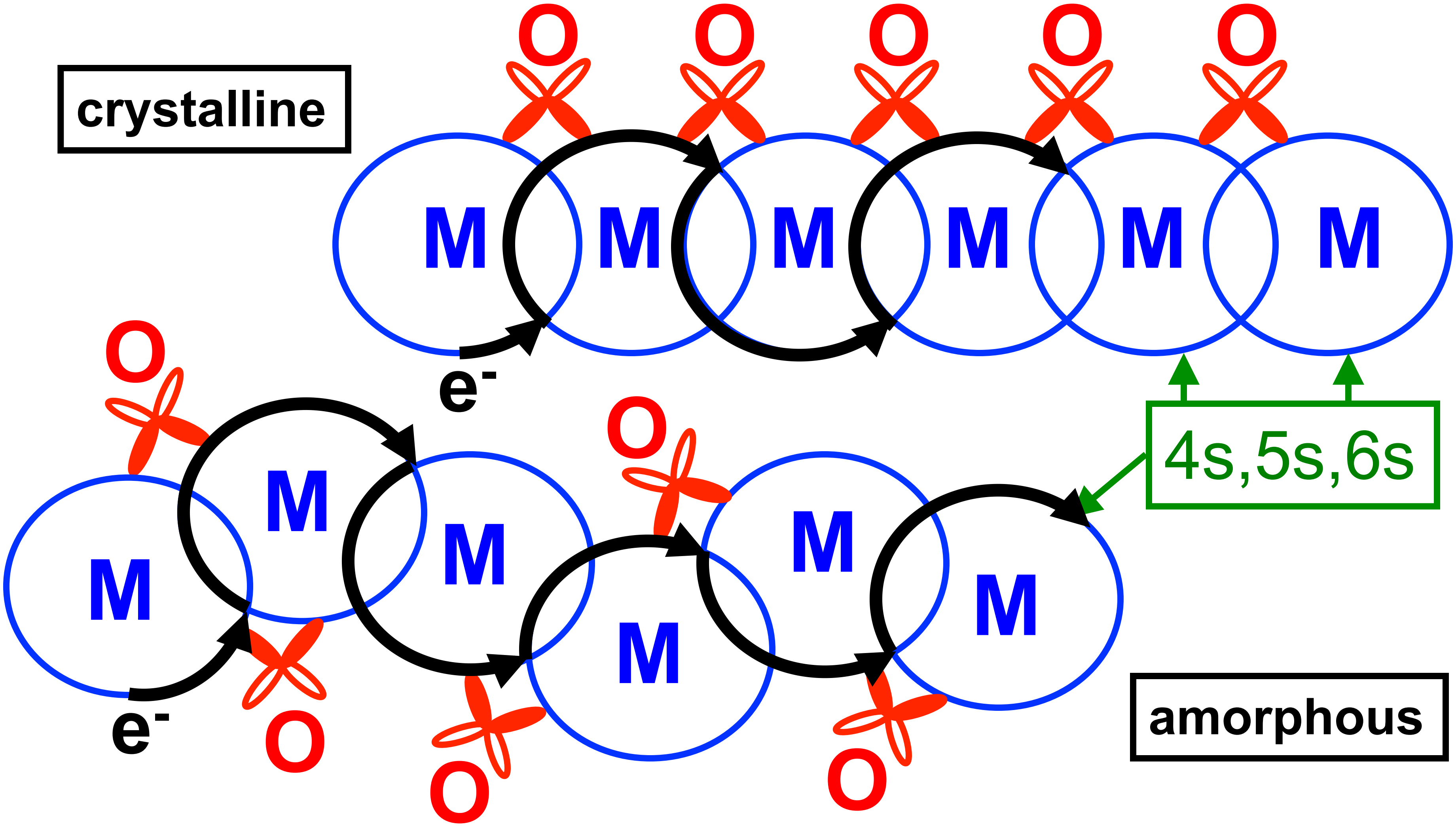


SnO_2 tetragonal rutile



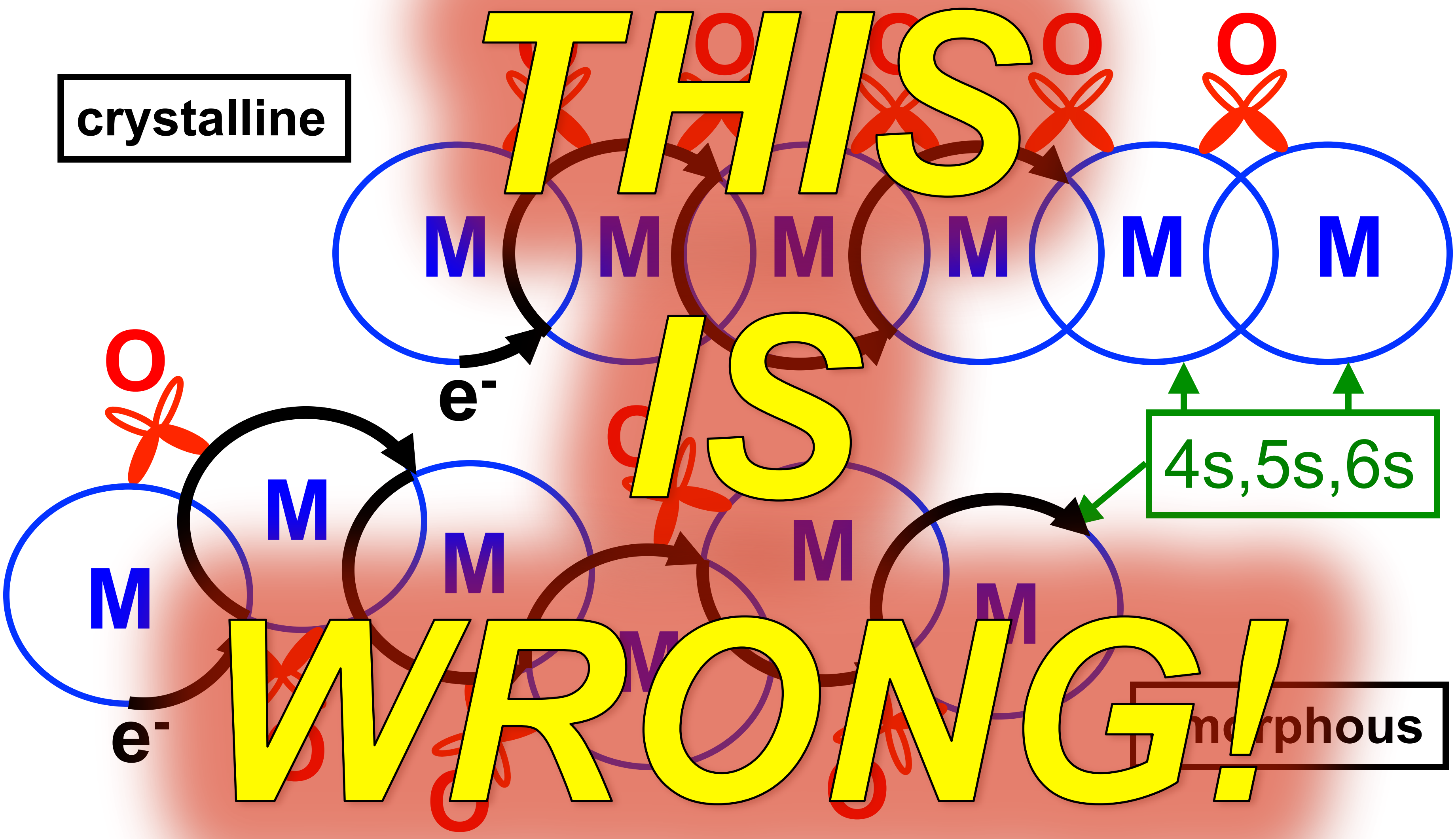
In_2O_3 cubic bixebyte

AOS



H. Hosono *et al.*, J. Non-Crystalline Solids 203, 334 (1996).

AOS



THIS IS WRONG!

H. Hosono *et al.*, J. Non-Crystalline Solids 203, 334 (1996).

Amorphous Semiconductor Mobility

$$\boxed{\mu_{drift} = \frac{n}{n + n_T}\mu_0}$$

n = free carriers

n_T = trapped carriers

μ_0 = diffusive (Brownian motion) mobility

$$\boxed{\mu_0 \text{ (IGZO)} \approx \mu_0 \text{ (a-Si:H)}}$$

Therefore, the Hosono picture is incorrect!

Amorphous Semiconductor Mobility

$$\mu_{drift} = \frac{n}{n + n_T} \mu_0$$

TRAPPING!

n_T (IGZO) < n_T (a-Si:H)

DISORDER (IGZO) < DISORDER (a-Si:H)

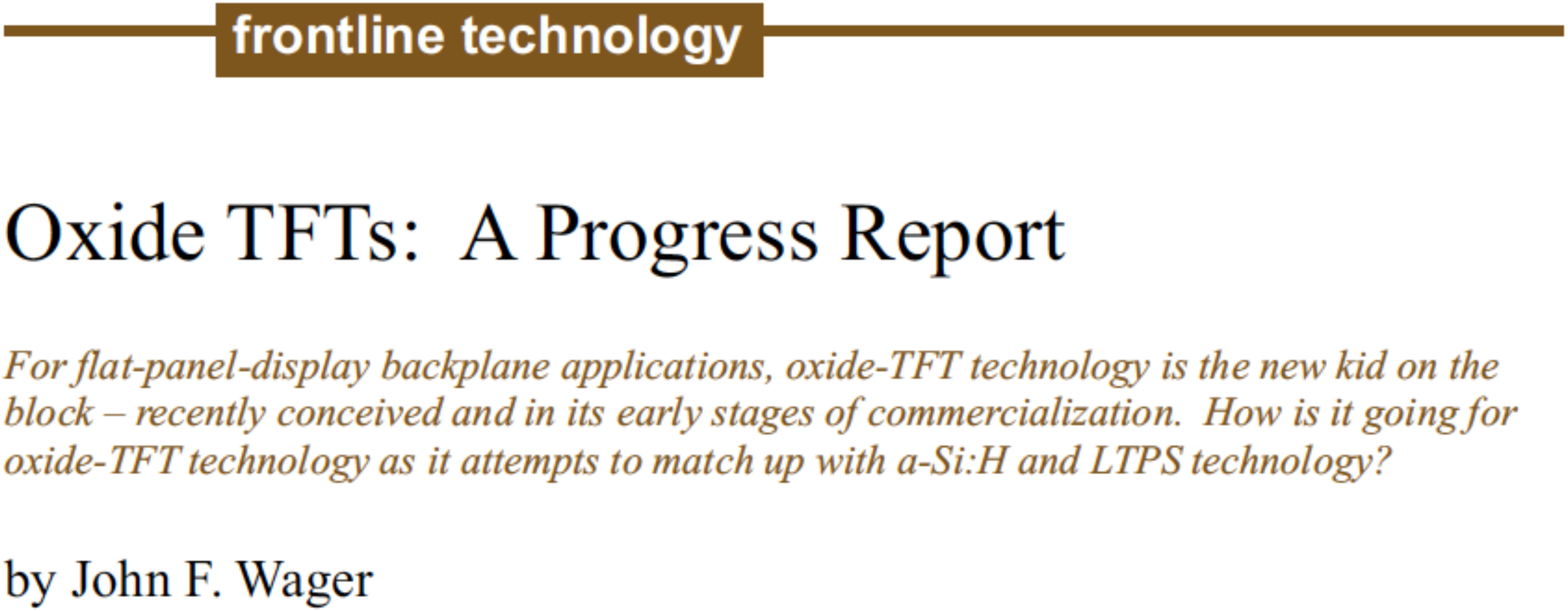
cation sublattice disorder

bond angle disorder

K.S. Stewart et al., JNCS 432B, 196 (2016).

Amorphous Semiconductor Transport Simulator, https://nanohub.org/resources/asts

Oxide TFTs



frontline technology

Oxide TFTs: A Progress Report

For flat-panel-display backplane applications, oxide-TFT technology is the new kid on the block – recently conceived and in its early stages of commercialization. How is it going for oxide-TFT technology as it attempts to match up with a-Si:H and LTPS technology?

by John F. Wager

J.F. Wager, Information Display, 1/16 (2016) 16-21.

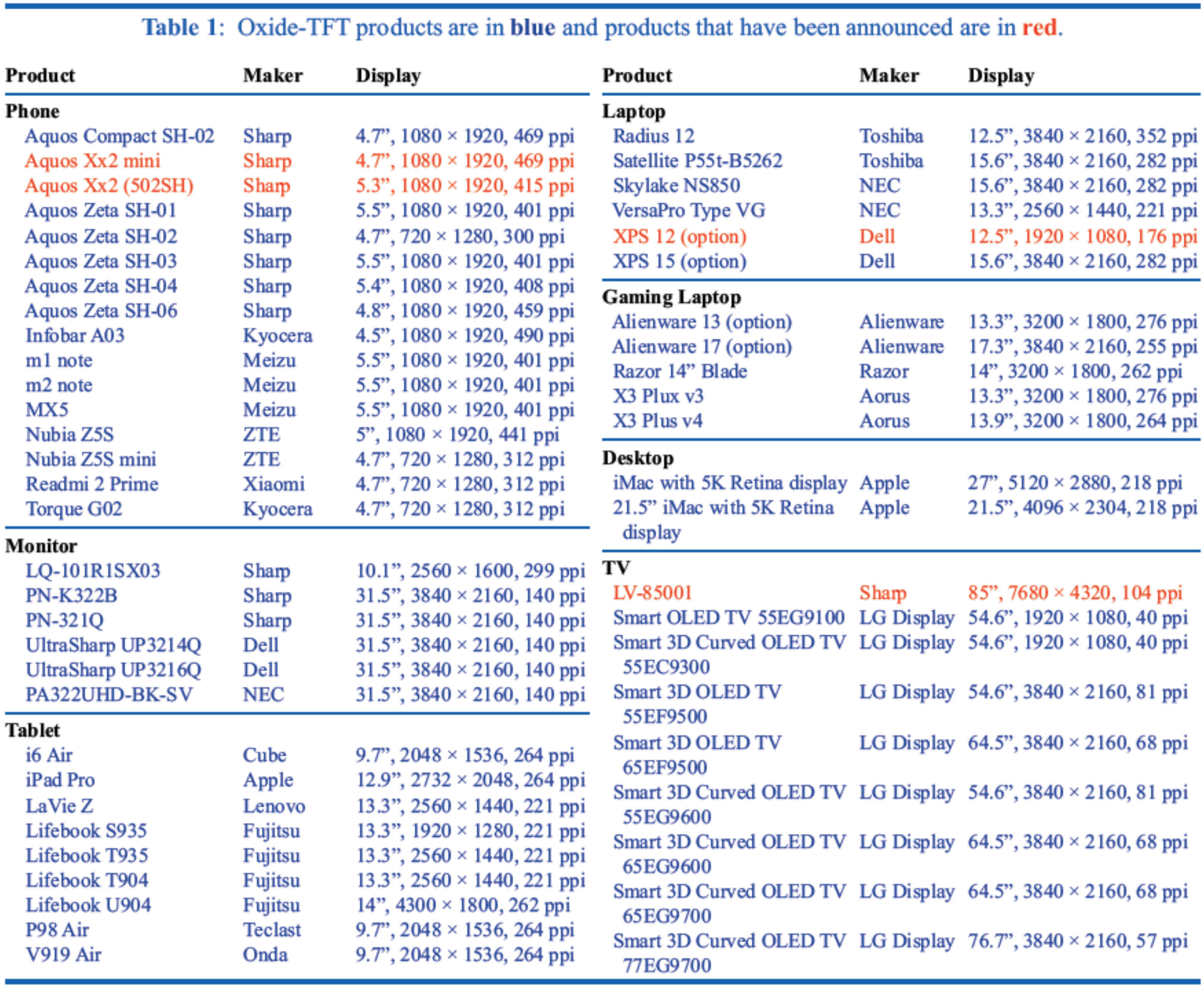


Table 1: Oxide-TFT products are in **blue** and products that have been announced are in **red**.

Product	Maker	Display
Phone		
Aquos Compact SH-02	Sharp	4.7”, 1080 × 1920, 469 ppi
Aquos Xx2 mini	Sharp	4.7”, 1080 × 1920, 469 ppi
Aquos Xx2 (502SH)	Sharp	5.3”, 1080 × 1920, 415 ppi
Aquos Zeta SH-01	Sharp	5.5”, 1080 × 1920, 401 ppi
Aquos Zeta SH-02	Sharp	4.7”, 720 × 1280, 300 ppi
Aquos Zeta SH-03	Sharp	5.5”, 1080 × 1920, 401 ppi
Aquos Zeta SH-04	Sharp	5.4”, 1080 × 1920, 408 ppi
Aquos Zeta SH-06	Sharp	4.8”, 1080 × 1920, 459 ppi
Infobar A03	Kyocera	4.5”, 1080 × 1920, 490 ppi
m1 note	Meizu	5.5”, 1080 × 1920, 401 ppi
m2 note	Meizu	5.5”, 1080 × 1920, 401 ppi
MX5	Meizu	5.5”, 1080 × 1920, 401 ppi
Nubia Z5S	ZTE	5”, 1080 × 1920, 441 ppi
Nubia Z5S mini	ZTE	4.7”, 720 × 1280, 312 ppi
Readmi 2 Prime	Xiaomi	4.7”, 720 × 1280, 312 ppi
Torque G02	Kyocera	4.7”, 720 × 1280, 312 ppi
Monitor		
LQ-101R1SX03	Sharp	10.1”, 2560 × 1600, 299 ppi
PN-K322B	Sharp	31.5”, 3840 × 2160, 140 ppi
PN-321Q	Sharp	31.5”, 3840 × 2160, 140 ppi
UltraSharp UP3214Q	Dell	31.5”, 3840 × 2160, 140 ppi
UltraSharp UP3216Q	Dell	31.5”, 3840 × 2160, 140 ppi
PA322UHD-BK-SV	NEC	31.5”, 3840 × 2160, 140 ppi
Tablet		
i6 Air	Cube	9.7”, 2048 × 1536, 264 ppi
iPad Pro	Apple	12.9”, 2732 × 2048, 264 ppi
LaVie Z	Lenovo	13.3”, 2560 × 1440, 221 ppi
Lifebook S935	Fujitsu	13.3”, 1920 × 1280, 221 ppi
Lifebook T935	Fujitsu	13.3”, 2560 × 1440, 221 ppi
Lifebook T904	Fujitsu	13.3”, 2560 × 1440, 221 ppi
Lifebook U904	Fujitsu	14”, 4300 × 1800, 262 ppi
P98 Air	Teclast	9.7”, 2048 × 1536, 264 ppi
V919 Air	Onda	9.7”, 2048 × 1536, 264 ppi
Laptop		
Radius 12	Toshiba	12.5”, 3840 × 2160, 352 ppi
Satellite P55t-B5262	Toshiba	15.6”, 3840 × 2160, 282 ppi
Skylake NS850	NEC	15.6”, 3840 × 2160, 282 ppi
VersaPro Type VG	NEC	13.3”, 2560 × 1440, 221 ppi
XPS 12 (option)	Dell	12.5”, 1920 × 1080, 176 ppi
XPS 15 (option)	Dell	15.6”, 3840 × 2160, 282 ppi
Gaming Laptop		
Alienware 13 (option)	Alienware	13.3”, 3200 × 1800, 276 ppi
Alienware 17 (option)	Alienware	17.3”, 3840 × 2160, 255 ppi
Razor 14” Blade	Razor	14”, 3200 × 1800, 262 ppi
X3 Plux v3	Aorus	13.3”, 3200 × 1800, 276 ppi
X3 Plus v4	Aorus	13.9”, 3200 × 1800, 264 ppi
Desktop		
iMac with 5K Retina display	Apple	27”, 5120 × 2880, 218 ppi
21.5” iMac with 5K Retina display	Apple	21.5”, 4096 × 2304, 218 ppi
TV		
LV-85001	Sharp	85”, 7680 × 4320, 104 ppi
Smart OLED TV 55EG9100	LG Display	54.6”, 1920 × 1080, 40 ppi
Smart 3D Curved OLED TV 55EC9300	LG Display	54.6”, 1920 × 1080, 40 ppi
Smart 3D OLED TV 55EF9500	LG Display	54.6”, 3840 × 2160, 81 ppi
Smart 3D OLED TV 65EF9500	LG Display	64.5”, 3840 × 2160, 68 ppi
Smart 3D Curved OLED TV 55EG9600	LG Display	54.6”, 3840 × 2160, 81 ppi
Smart 3D Curved OLED TV 65EG9600	LG Display	64.5”, 3840 × 2160, 68 ppi
Smart 3D Curved OLED TV 65EG9700	LG Display	64.5”, 3840 × 2160, 68 ppi
Smart 3D Curved OLED TV 77EG9700	LG Display	76.7”, 3840 × 2160, 57 ppi

Oxide TFTs

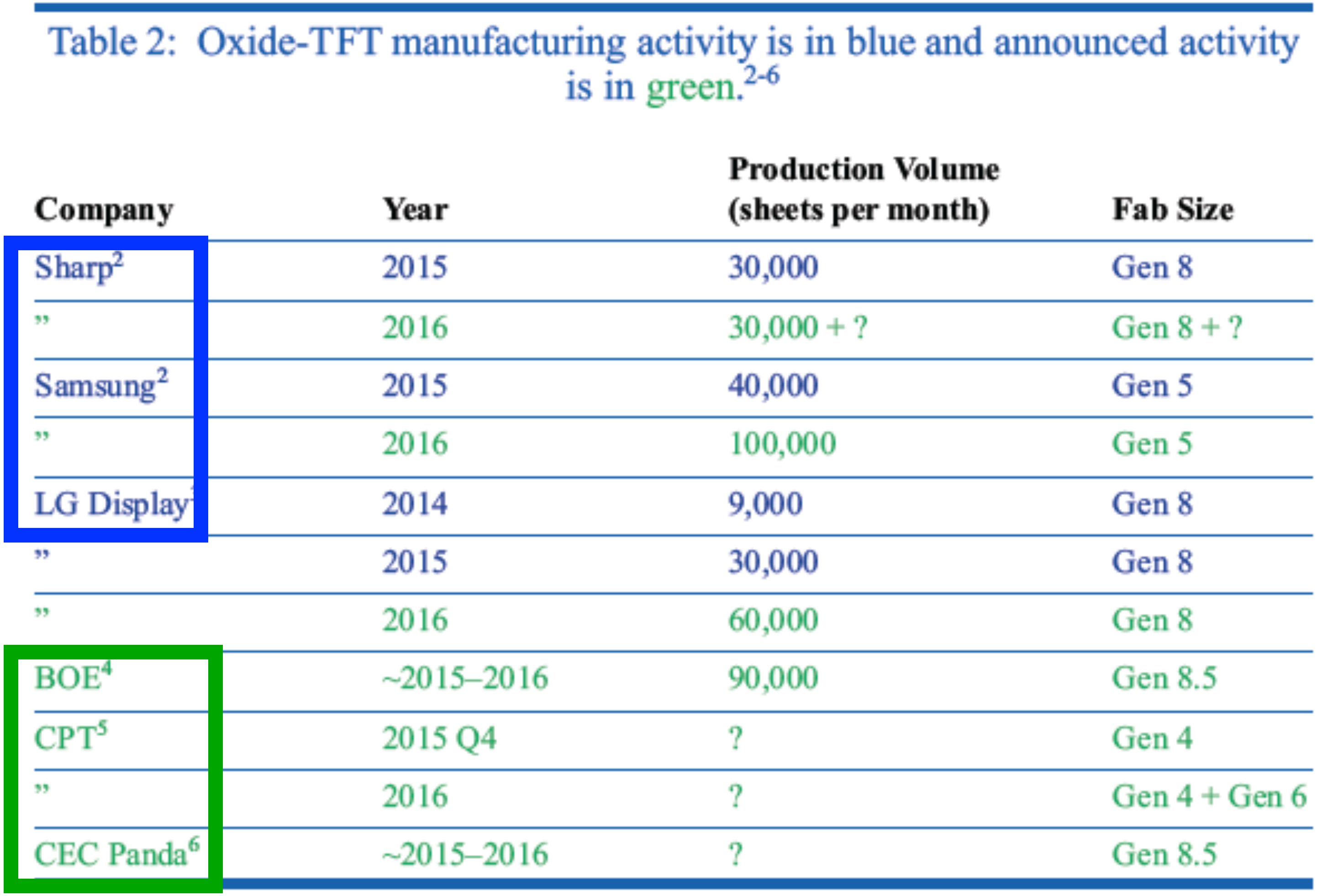


Table 2: Oxide-TFT manufacturing activity is in blue and announced activity is in green.[2-6]

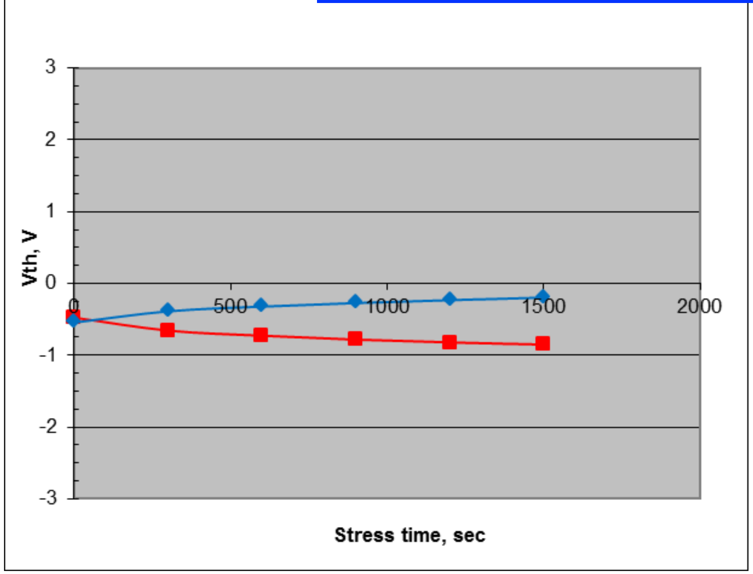
Company	Year	Production Volume (sheets per month)	Fab Size
Sharp[2]	2015	30,000	Gen 8
”	2016	30,000 + ?	Gen 8 + ?
Samsung[2]	2015	40,000	Gen 5
”	2016	100,000	Gen 5
LG Display	2014	9,000	Gen 8
”	2015	30,000	Gen 8
”	2016	60,000	Gen 8
BOE[4]	~2015–2016	90,000	Gen 8.5
CPT[5]	2015 Q4	?	Gen 4
”	2016	?	Gen 4 + Gen 6
CEC Panda[6]	~2015–2016	?	Gen 8.5

Oxide TFTs

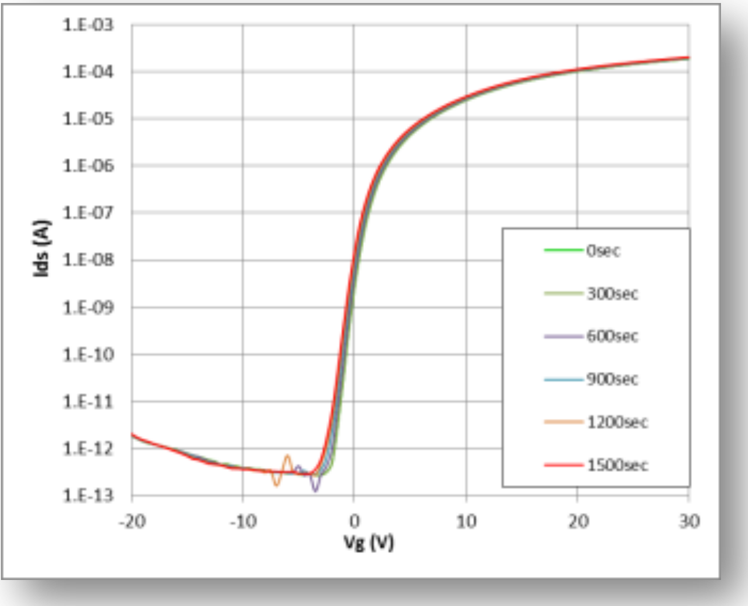
TFT performance:

Mobility: ~12 cm^{2}V^{-1}s^{-1}
I_{ON}/I_{OFF}: > 10^8

S: ~0.45 V/decade
V_{ON}: ~0 V



PBTS NBTS
ΔV_{th} 0.35 V -0.38 V
P/NBTS (60 °C, ±30 V, 1500 s)



ΔV_{th} = -0.58 V @ 1000 nit
NBIS (60 °C, -30 V, 1500 s)

Courtesy Applied Materials

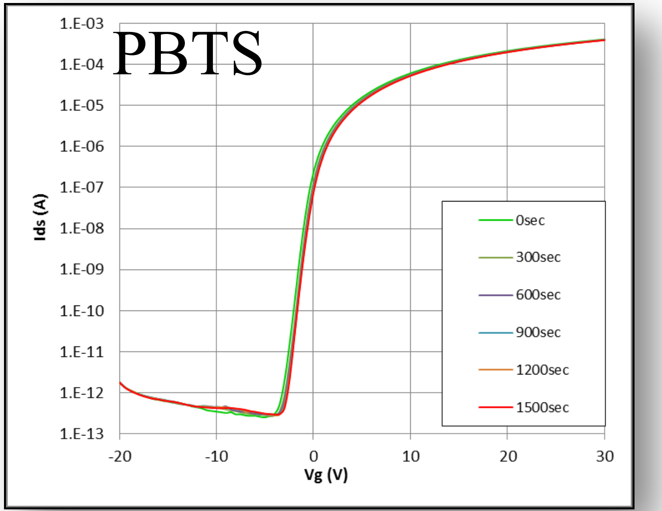
Oxide TFTs

Fig. 1: *This rotary target array consists of 12 Gen 8.5 IGZO sputter targets (a*
tured at left) installed in an Applied Materials PIVOT-sputtering system. (For
note the person standing in front of the system.) Image courtesy Applied Mate

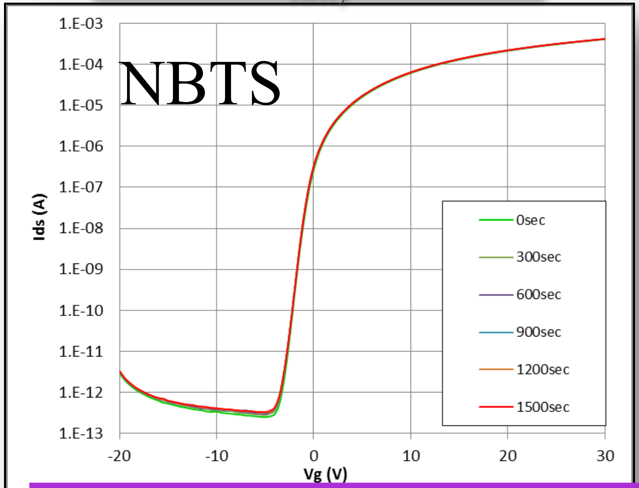
!

Courtesy Applied Materials

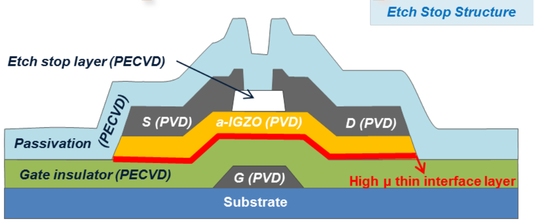
Oxide TFTs (DAL)

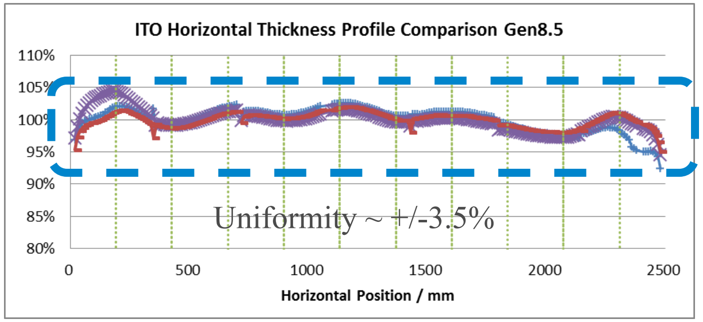


IZO (5 nm) + IGZO (60 nm)



Courtesy Applied Materials





Thin layer capability

Dual layer approach: strong potential for high mobility oxide TFT:

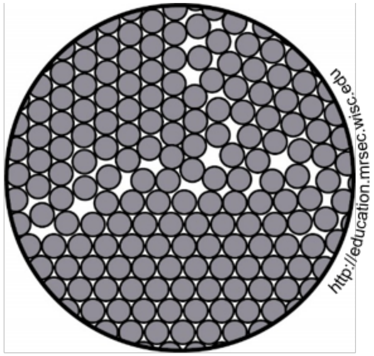
- Simple mobility modification via interface layer thickness control
- V_{th} control by back channel tuning
- Excellent bias stress stability

IZO Interface thickness (nm)	Mobility ($cm^2V^{-1}s^{-1}$)	S (V/decade)	V_{th} (V)	PBTS* (V)	NBTS* (V)
5	38	0.32	-1.5	0.51	-0.11
7.5	47	0.41	-2.0	0.38	0.10
10	62	0.41	-2.9	0.35	-0.03

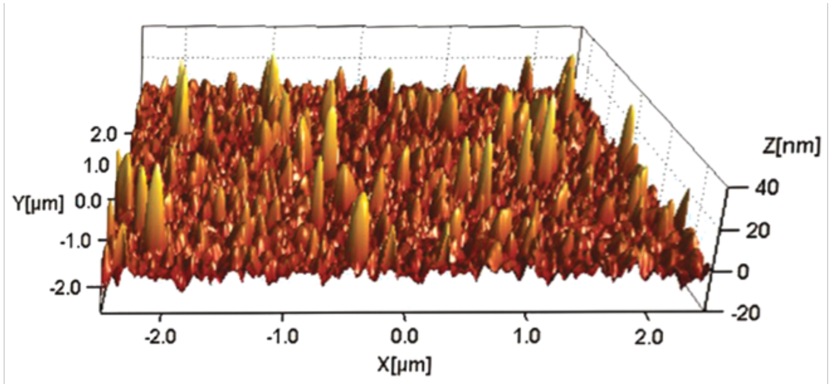
*Stress Conditions : 60 °C, ±30 V, 1500 s

(iii) Future?

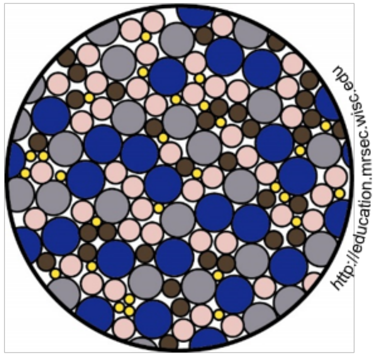
Amorphous Metal Thin Film Surfaces



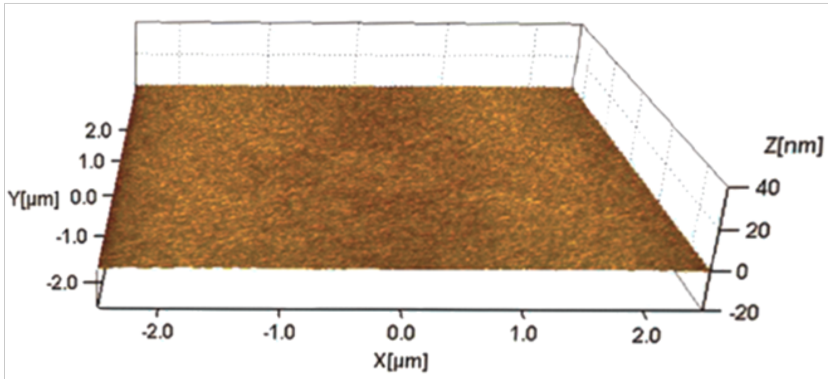
Crystalline



RMS Roughness > 1-5nm

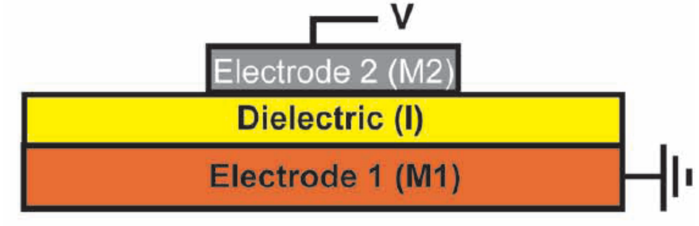


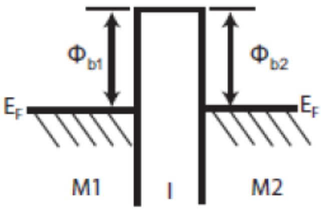
Amorphous



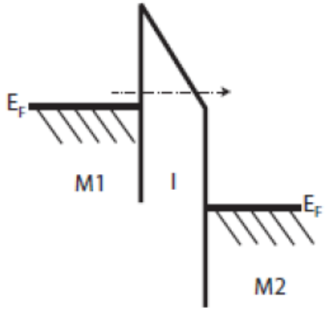
RMS Roughness < 1nm

Metal-Insulator-Metal (MIM) Diode





(b)



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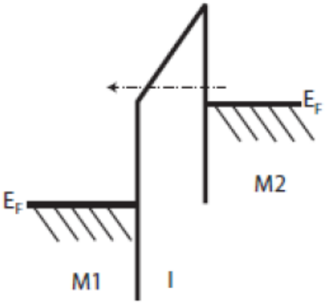

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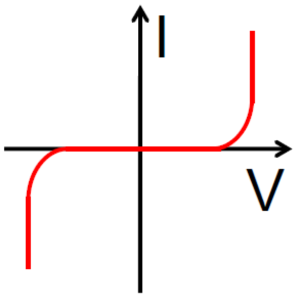
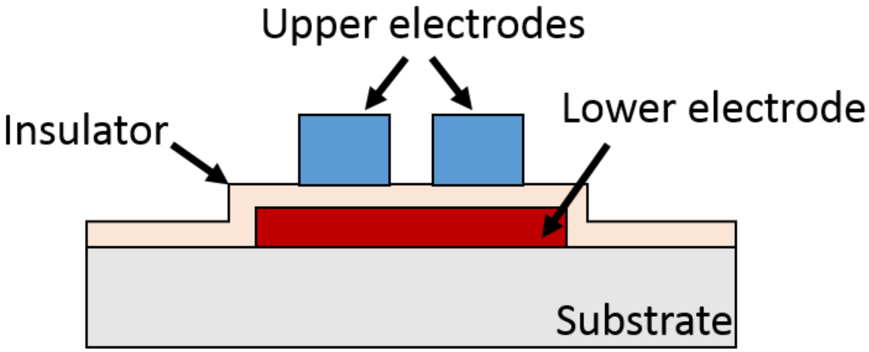
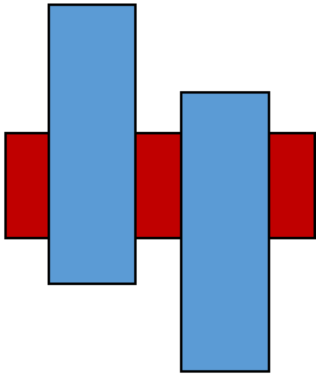


Fowler-Nordheim tunneling

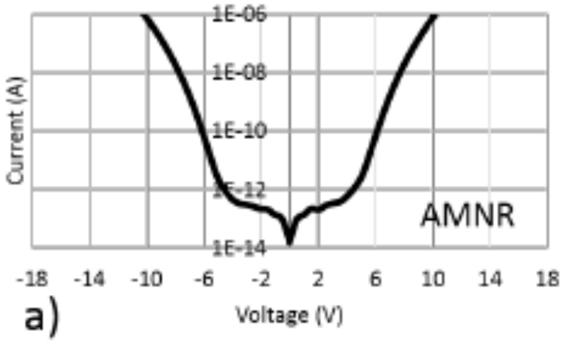
Amorphous Metal Non-Linear Resistors

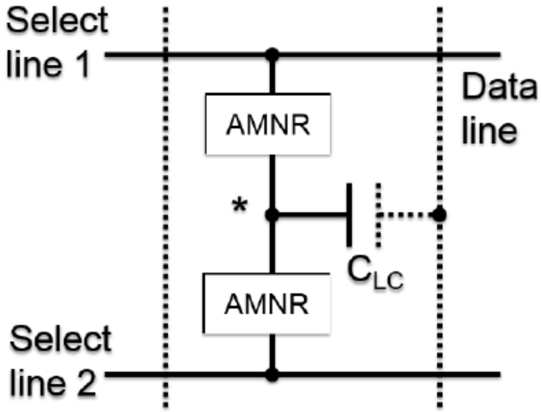


a)



b)





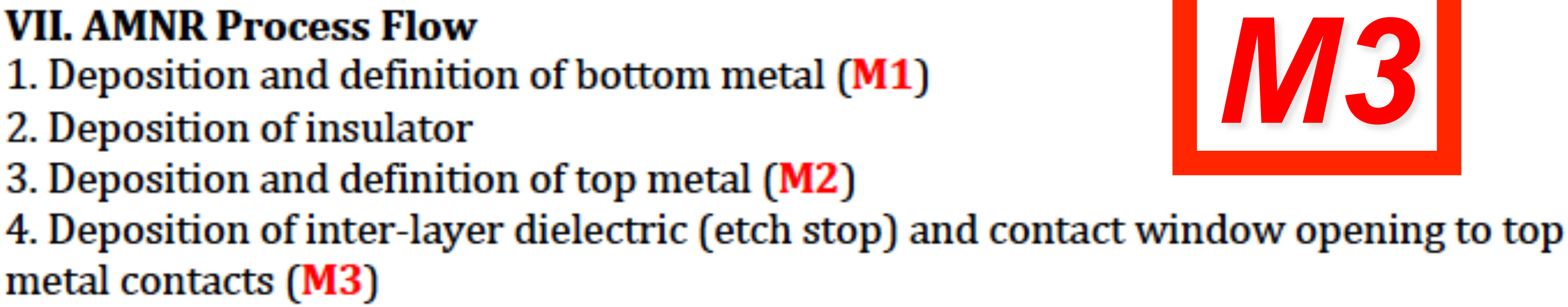
*Virtual ground

S. Muir et al., Information Display, 1/16 (2016) 22-27.

Amorphous Metal Non-Linear Resistors

VII. AMNR TFDs

M3

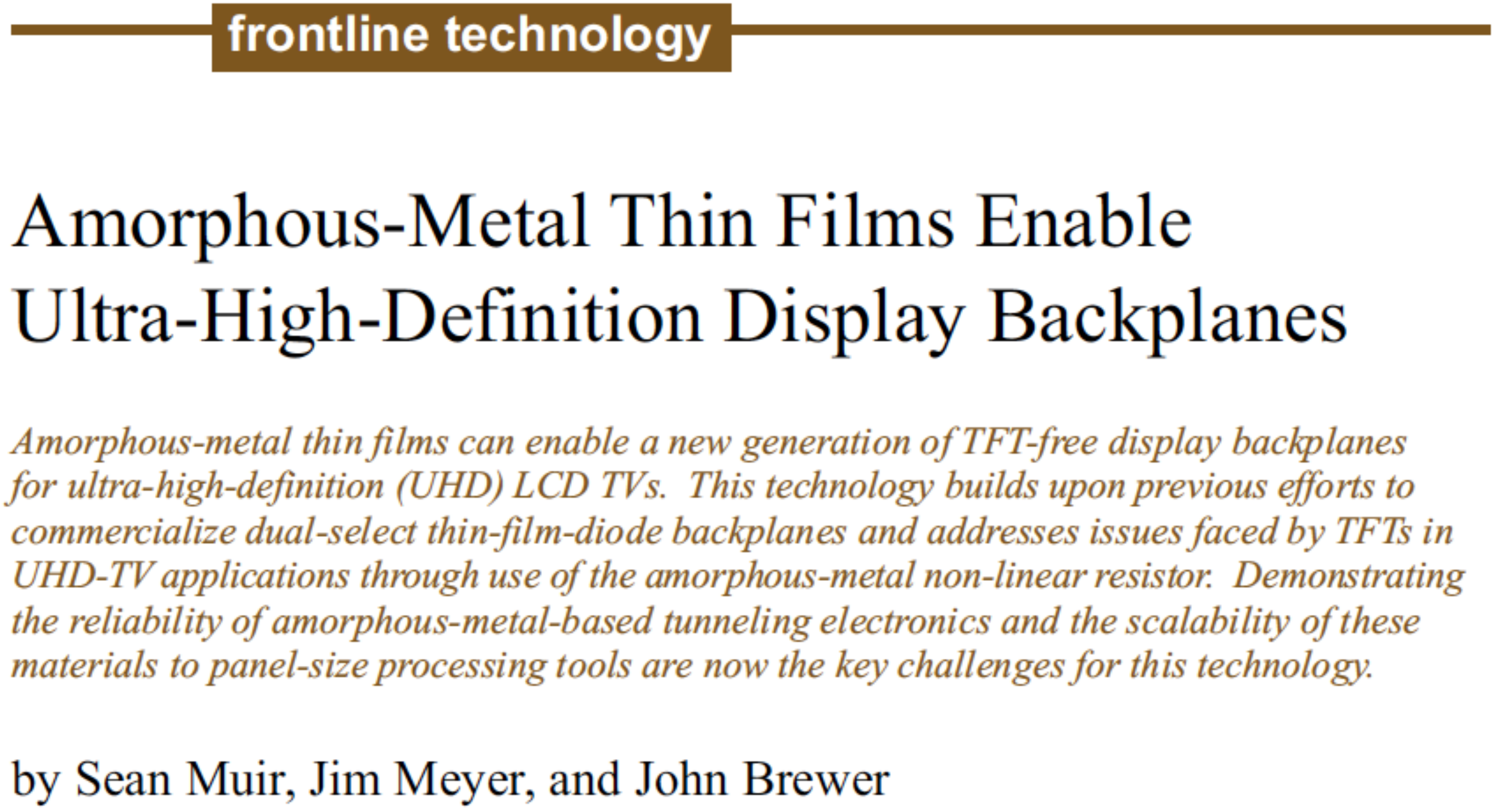


VII. AMNR Process Flow

1. Deposition and definition of bottom metal (**M1**)
2. Deposition of insulator
3. Deposition and definition of top metal (**M2**)
4. Deposition of inter-layer dielectric (etch stop) and contact window opening to top metal contacts (**M3**)

- *Ultra-simple process*
- *Low temperature sensitivity*
- *Low light sensitivity*
- *Superior to Poole-Frenkel TFDs*

Amorphous Metal Non-Linear Resistors



frontline technology

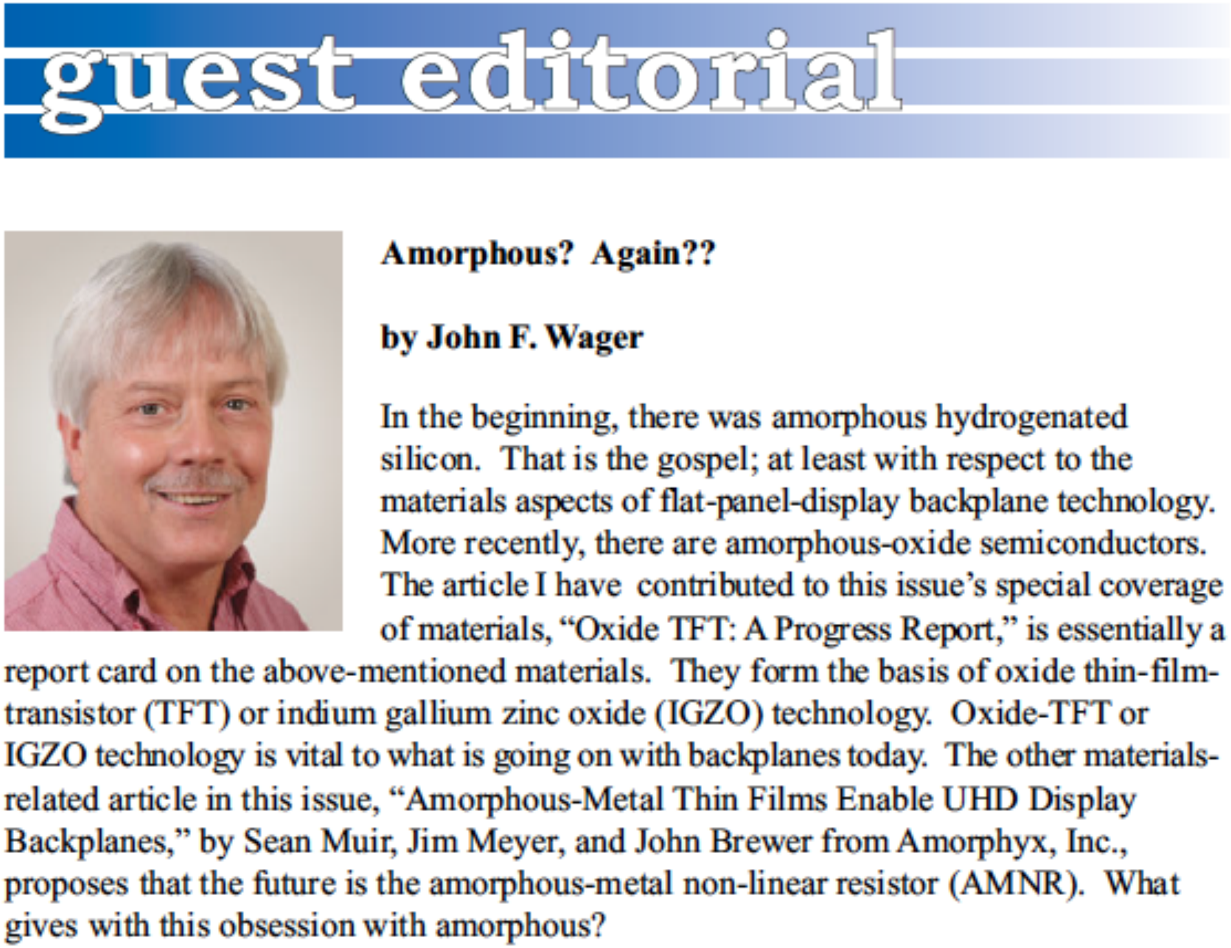
Amorphous-Metal Thin Films Enable Ultra-High-Definition Display Backplanes

Amorphous-metal thin films can enable a new generation of TFT-free display backplanes for ultra-high-definition (UHD) LCD TVs. This technology builds upon previous efforts to commercialize dual-select thin-film-diode backplanes and addresses issues faced by TFTs in UHD-TV applications through use of the amorphous-metal non-linear resistor. Demonstrating the reliability of amorphous-metal-based tunneling electronics and the scalability of these materials to panel-size processing tools are now the key challenges for this technology.

by Sean Muir, Jim Meyer, and John Brewer

S. Muir et al., Information Display, 1/16 (2016) 22-27.

Amorphous Metal Non-Linear Resistors



guest editorial

Amorphous? Again??

by John F. Wager

In the beginning, there was amorphous hydrogenated silicon. That is the gospel; at least with respect to the materials aspects of flat-panel-display backplane technology. More recently, there are amorphous-oxide semiconductors. The article I have contributed to this issue's special coverage of materials, "Oxide TFT: A Progress Report," is essentially a report card on the above-mentioned materials. They form the basis of oxide thin-film-transistor (TFT) or indium gallium zinc oxide (IGZO) technology. Oxide-TFT or IGZO technology is vital to what is going on with backplanes today. The other materials-related article in this issue, "Amorphous-Metal Thin Films Enable UHD Display Backplanes," by Sean Muir, Jim Meyer, and John Brewer from Amorphyx, Inc., proposes that the future is the amorphous-metal non-linear resistor (AMNR). What gives with this obsession with amorphous?

J.F. Wager, Information Display, 1/16 (2016) 4,43.

Conclusions

(i) Past: a-Si:H

(ii) Present: a-Si:H → LTPS & IGZO

(iii) Future: AMNR TFD's?

- ✓ Insulator depostion via PECVD or ALD?
- ✓ Peformance/stability/reliability/scalability?